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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/975,293	Applicant(s) YEUNG ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1, 3-6, 12, 14, 15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka; Hideto et al. (US 4730320 A, hereafter referred to as Hidaka) in view of Chen; Chin L. (US 4464753 A).

35 U.S.C. 103(a) rejection of claims 1, 14 and 15.

Hidaka teaches a first circuit configured to generate a first syndrome signal in response to a read data signal and a read parity signal (Syndrome Generator 5 in Figure 6 of Hidaka is a first circuit configured to generate a first syndrome signal f in response to a read data signal d and a read parity signal e; Note: Read Check Bit Generator 4 produces a read parity signal e whereby Syndrome Generator 5 is configured to generate syndrome signal f in response to a read data signal d from Memory 3 and a read parity signal e from Read Check Bit Generator 4); a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal and a bypass signal (Syndrome Output Circuit 70 in Figure 6 of Hidaka is a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal f and a bypass signal TE; Note: col. 7, lines 60-68 of Hidaka teaches that in normal operation Syndrome Output bypass Circuit 70 generates an output, second syndrome signal f, and during data bit test mode Syndrome Output bypass Circuit 70 is configured to bypass the Syndrome Decoder and instead outputs second syndrome signal f to other circuitry); and a second circuit configured to (i) detect an error when bits of said second syndrome signal are not all the same state and (ii) generate an error location signal in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal (Syndrome Decoder 6 in Hidaka is a second circuit configured to detect an error when bits of said second syndrome signal are not all the same state and generate an error location signal g output to Data Correction Circuit 7 in response to said second syndrome signal from Syndrome Output bypass Circuit 70, wherein said error location

signal is generated in response to fewer than all of said bits of said second syndrome signal; Note: if all the syndromes are zero, then inherently there is no error and only the non-zero syndromes are necessary to generate error locations, hence the error location signal is generated in response to the non-zero syndromes, i.e., the error location signal is generated in response to fewer than all of said bits of said second syndrome signal when there exist non-zero syndromes).

However Hidaka does not explicitly teach the specific use of a single error correction (SEC) decoder typically used in memory devices.

Chen, in an analogous art, teaches use of a single error correction (SEC) decoder typically used in memory devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hidaka with the teachings of Chen by including use of a single error correction (SEC) decoder typically used in memory devices. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a single error correction (SEC) decoder typically used in memory devices would have provided the ability to correct errors in a memory package even when a single chip in the memory package fails (col. 1, lines 18-22, Chen).

35 U.S.C. 103(a) rejection of claim 3.

Data Correction Circuit 7 in Figure 6 of Hidaka is configured to present said read data and parity signals at an output when no error is detected in said read data and parity

signals. Note: Data Correction Circuit 7 is configured to present said read data and parity signals at an output regardless of whether errors are found or not.

35 U.S.C. 103(a) rejection of claim 4.

Figure 6 of Hidaka teaches a memory circuit configured to (i) receive a data input signal input on line 1 and a parity input signal from Write Check Bit Generator 2 during a write operation and (ii) present said read data d and parity signals c during a read operation.

35 U.S.C. 103(a) rejection of claim 5.

Chen teaches Single Error Correction with Double Error Detection (SEC/DED).

35 U.S.C. 103(a) rejection of claim 6.

Data Correction Circuit 7 in Figure 6 of Hidaka is configured to present said read data and parity signals at an output when no error is detected in said read data and parity signals. Note: Data Correction Circuit 7 is configured to present said read data and parity signals at an output regardless of whether errors are found or not.

35 U.S.C. 103(a) rejection of claims 12 and 17.

Syndrome Output Circuit 70 in Figure 6 of Hidaka is a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal f and a bypass signal TE; Note: col. 7, lines 60-68 of Hidaka teaches that in normal operation Syndrome Output bypass Circuit 70 generates an output, second syndrome signal f,

and during data bit test mode Syndrome Output bypass Circuit 70 is configured to bypass the Syndrome Decoder and instead outputs second syndrome signal f to other circuitry.

35 U.S.C. 103(a) rejection of claim 18.

Chen teaches Single Error Correction with Double Error Detection (SEC/DED).

35 U.S.C. 103(a) rejection of claims 19 and 20.

Data Correction Circuit 7 in Figure 6 of Hidaka is configured to present said read data and parity signals at an output when no error is detected in said read data and parity signals. Note: Data Correction Circuit 7 is configured to present said read data and parity signals at an output regardless of whether errors are found or not.

35 U.S.C. 103(a) rejection of claim 21.

Syndrome Output Circuit 70 in Figure 6 of Hidaka is a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal f and a bypass signal TE; Note: col. 7, lines 60-68 of Hidaka teaches that in normal operation Syndrome Output bypass Circuit 70 generates an output, second syndrome signal f, and during data bit test mode Syndrome Output bypass Circuit 70 is configured to bypass the Syndrome Decoder and instead outputs second syndrome signal f to other circuitry.

3. Claims 2, 8, 11, 13, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka; Hideto et al. (US 4730320 A, hereafter referred to as Hidaka) in view of Chen; Chin L. (US 4464753 A) in further view of Stiffler; Jack J. (US 4736376 A).

35 U.S.C. 103(a) rejection of claim 2, 13 and 16.

Hidaka and Chen substantially teaches the claimed invention described in claims 1, 14 and 15 (as rejected above).

However Hidaka and Chen does not explicitly teach the specific use of first syndrome signals being at 1 when there is no error .

Stiffler, in an analogous art, teaches all of said bits of said first syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1 (col. 9, lines 52-55 in Stiffler teach that d1="1" or d2="1" indicates an error; col. 12, lines 59-61 in Stiffler teach that [c1…c4] are all "true"="1" when d1="0" and d2="1" indicating an error). Note: The Examiner asserts that syndromes are usually 0 when there is no error, however; using an inverter to convert them to 1 when there is no error, as Stiffler does not deviate from the Prior Art since the choice of all zeros representing an error is convention.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hidaka and Chen with the teachings of Stiffler by including use of first syndrome signals being at 1 when there is no error. This modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that use of first syndrome signals being at 1 when there is no error would have recognized that using all ones to represent no error is substantially identical to using all zeros to represent no errors and is merely an alternative convention.

35 U.S.C. 103(a) rejection of claim 8.

Figure 8 in Stiffler teaches second syndrome signal [h1...h4] is produced using non-inverting exclusive-Or gates, which is a type selected from the group consisting of (i) **non-inverting exclusive-OR gates**, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

35 U.S.C. 102(b) rejection of claim 11.

Figure 7 in Stiffler teaches first syndrome signal [c1...c4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, (iii) **inverting exclusive-OR gates**, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting

exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate. Note: Figure 7 in Stiffler teaches first syndrome signal [e1...e4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type selected from the group consisting of (i) **non-inverting exclusive-OR gates**, (ii) **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

35 U.S.C. 103(a) rejection of claim 22.

Hidaka teaches a first circuit configured to generate a first syndrome signal in response to a read data signal and a read parity signal (Syndrome Generator 5 in Figure 6 of Hidaka is a first circuit configured to generate a first syndrome signal f in response to a read data signal d and a read parity signal e; Note: Read Check Bit Generator 4 produces a read parity signal e whereby Syndrome Generator 5 is configured to generate syndrome signal f in response to a read data signal d from Memory 3 and a read parity signal e from Read Check Bit Generator 4); a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal and a

bypass signal (Syndrome Output Circuit 70 in Figure 6 of Hidaka is a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal f and a bypass signal TE; Note: col. 7, lines 60-68 of Hidaka teaches that in normal operation Syndrome Output bypass Circuit 70 generates an output, second syndrome signal f, and during data bit test mode Syndrome Output bypass Circuit 70 is configured to bypass the Syndrome Decoder and instead outputs second syndrome signal f to other circuitry); and a second circuit configured to (i) detect an error when bits of said second syndrome signal are not all the same state and (ii) generate an error location signal in response to said second syndrome signal, wherein said error location signal (i) is generated in response to fewer than all of said bits of said second syndrome signal (Syndrome Decoder 6 in Hidaka is a second circuit configured to detect an error when bits of said second syndrome signal are not all the same state and generate an error location signal g output to Data Correction Circuit 7 in response to said second syndrome signal from Syndrome Output bypass Circuit 70, wherein said error location signal is generated in response to fewer than all of said bits of said second syndrome signal; Note: if all the syndromes are zero, then inherently there is no error and only the non-zero syndromes are necessary to generate error locations, hence the error location signal is generated in response to the non-zero syndromes, i.e., the error location signal is generated in response to fewer than all of said bits of said second syndrome signal when there exist non-zero syndromes).

However Hidaka does not explicitly teach the specific use of a single error correction (SEC) decoder typically used in memory devices.

Chen, in an analogous art, teaches use of a single error correction (SEC) decoder typically used in memory devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hidaka with the teachings of Chen by including use of a single error correction (SEC) decoder typically used in memory devices. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a single error correction (SEC) decoder typically used in memory devices would have provided the ability to correct errors in a memory package even when a single chip in the memory package fails (col. 1, lines 18-22, Chen).

However Hidaka and Chen does not explicitly teach the specific use of first syndrome signals being at 1 when there is no error .

Stiffler, in an analogous art, teaches all of said bits of said first syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1 (col. 9, lines 52-55 in Stiffler teach that d1="1" or d2="1" indicates an error; col. 12, lines 59-61 in Stiffler teach that [c1...c4] are all "true"="1" when d1="0" and d2="1" indicating an error). Note: The Examiner asserts that syndromes are usually 0 when there is no error, however; using an inverter to convert them to 1 when there is no error, as Stiffler does not deviate from the Prior Art since the choice of all zeros representing an error is convention. Note: Figure 7 in Stiffler teaches first syndrome signal [c1...c4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate, which is a type

selected from the group consisting of i. non-inverting exclusive-OR gates, ii. **non-inverting exclusive-OR gates with an output inverted by a NOT gate**, iii. **inverting exclusive-OR gates**, iv. inverting exclusive-OR gates with an output inverted by a NOT gate, v. non-inverting exclusive-NOR gates, vi. inverting exclusive-NOR gates, vii. non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and viii. inverting exclusive-NOR gates with an output inverted by a NOT gate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hidaka and Chen with the teachings of Stiffler by including use of first syndrome signals being at 1 when there is no error. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of first syndrome signals being at 1 when there is no error would have recognized that using all ones to represent no error is substantially identical to using all zeros to represent no errors and is merely an alternative convention.

4. Claims 7, 9, 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka; Hideto et al. (US 4730320 A, hereafter referred to as Hidaka), Chen; Chin L. (US 4464753 A) and Stiffler; Jack J. (US 4736376 A).

35 U.S.C. 103(a) rejection of claim 7.

Stiffler substantially teaches the claimed invention described in claims 1-6 (as rejected above). In addition, col. 10, lines 6-8 in Stiffler teach the 2nd Stage Syndrome Generator

444 in Figure 4 of Stiffler produces the inverse half [i1...i4] of the second syndrome bits [h1...h4].

However Hidaka, Chen and Stiffler does not explicitly teach the specific use of inverting each of said bits of said second syndrome signal **in the second circuit**.

The Examiner asserts that Figure 4 of Stiffler is a block diagram for establishing the logical layout of the design and that the actual circuit layout is based on obvious engineering design choices, hence an embodiment of the design in the Stiffler patent including 2nd Stage Syndrome Generator 444 in Figure 4 as part of the second circuit, 1st Stage Syndrome Decoder 458, is an obvious engineering design choice based on actual design requirements such as cost, feasibility, available space, stray capacitance, etc.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hidaka, Chen and Stiffler by including 2nd Stage Syndrome Generator 444 in Figure 4 of Stiffler as part of the second circuit, 1st Stage Syndrome Decoder 458. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that including 2nd Stage Syndrome Generator 444 in Figure 4 as part of the second circuit, 1st Stage Syndrome Decoder 458 would have provided the opportunity to implement an embodiment of the circuit in Figure 4 of Stiffler based on obvious engineering design choice such as cost, feasibility, available space, stray capacitance, etc.

35 U.S.C. 103(a) rejection of claims 9 and 23.

Hidaka, Chen and Stiffler substantially teaches the claimed invention described in claims 1-9 (as rejected above). In addition, Stiffler teaches one or more OR gates (930, 936, 942 & 948 in Figure 9 and 1506 & 1510 in Figure 15 of Stiffler) configured to receive an inverse ([i1...i4] in Figure 9) of said second syndrome signal ([h1...h4] in Figure 9) and present said error detected signal (q1 and q2); one or more exclusive-OR gates configured to receive an inverse of said second syndrome signal and present an intermediate signal (col. 15, lines 23-43 in Stiffler teach that exclusive-OR gates 1202-1208 are configured to receive an inverse [i1...i4] of said second syndrome signal and present an intermediate signal [s1...s4]); one or more AND gates configured to present said single error signal in response to said error detected signal and said intermediate signal (intermediate signal [s1...s4] comprise parity for a stored word and are stored with the word in memory and upon reading the word are submitted to the decoder via 401 whereby [s1...s4]=[b17=b20]; Note: [b17=b20] are used to generate [c1...c4] and [e1...e4] in Figure 7, which are used to generate [h1...h4] and [i1...i4] in Figure 8 which are submitted to one or more AND gates 926-980 in Figure 9 to produce [j1...j4] and [l1...l4] which are used to produce said single error signal and said double error signal); and an AND gate configured to present said double error signal in response to said error detected signal and said intermediate signal (intermediate signal [s1...s4] comprise parity for a stored word and are stored with the word in memory and upon reading the word are submitted to the decoder via 401 whereby [s1...s4]=[b17=b20]; Note: [b17=b20] are used to generate [c1...c4] and [e1...e4] in Figure 7, which are used

to generate [h1...h4] and [i1...i4] in Figure 8 which are submitted to one or more AND gates 926-980 in Figure 9 to produce [j1...j4] and [l1...l4] which are used to produce said single error signal and said double error signal; Note: NAND gates 902-918 substantially invert output which is equivalent to ORing the inverse of the inputs).

However Hidaka, Chen and Stiffler does not explicitly teach the specific use of an AND gate configured to present said double error signal in response to said error detected signal and **an inverse** of said intermediate signal (Note: Stiffler teaches an AND gate configured to present said double error signal in response to said error detected signal and said intermediate signal, see previous paragraph, above).

The Examiner asserts that NAND gates 902-918 in Figure 9 substantially invert output, which is equivalent to ORing the inverse of the inputs; hence use of an inverted intermediate signal is substantially an equivalent embodiment. One of ordinary skill in the art at the time the invention was made would have been highly motivated to invert the intermediate signal based on obvious engineering design choices such as available circuitry, design layout, and intrinsic qualities of circuit components that effect overall efficiency and cost of circuitry.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hidaka, Chen and Stiffler by including use of an AND gate configured to present said double error signal in response to said error detected signal and **an inverse** of said intermediate signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an

AND gate configured to present said double error signal in response to said error detected signal and **an inverse** of said intermediate signal would have provided the opportunity to implement a substantially equivalent embodiment of the circuit of Figure 4 in Stiffler based on obvious engineering design choices such as available circuitry, design layout, and intrinsic qualities of circuit components that effect overall efficiency and cost of circuitry.

35 U.S.C. 103(a) rejection of claim 10.

Stiffler substantially teaches said single error signal comprises a multi-bit digital signal since the three bits, one each from NOR Gates 1620, 1436 and 1438 in Figures 14 and 16 are used to indicate correctable and uncorrectable errors, i.e., single and double errors.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133